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Molecular Electronics Division
WEST COAST DEPARTMENT
2420 Arnold Drive
Newbury Park, California

First
Quarterly Progress Report
On

ANALOG VOLTAGE TO DUTY CYCLE GENERATOR

March 15, 1966

J.P.L. Contract # 951306

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ANALOG VOLTAGE TO DUTY CYCLE GENERATOR

PROGRESS SUMMARY

System Functional Tests were made at Jet Propulsion Laboratory from January 12 through January 14, 1966. These tests indicated basic system feasibility and resulted in line and load regulation data which was within expected limits. Some compatability problems were noted and either completely or partially corrected. The problems which were partially corrected have been studied and appropriate redesign steps taken.

During this design and evaluation phase of the program an unrelated product development at Westinghouse has resulted in a production process for tantalum resistors. This process can easily be extended to produce tantalum capacitors as well. These components provide much greater design flexibility and prompted re-evaluation of our design approach. The results of this study were presented to Jet Propulsion Laboratory in a "Summary of Design Alternatives for the Analog Voltage to Duty Cycle Generator" which is reproduced within this report. References discussing the capacitor process were also provided, and are contained herein.

Design effort will continue on both basic approachs until the thin film components have been proven. This will not involve a significant increase in effort until the mask making phase, by which time the thin film components should be fully evaluated.

A program schedule has been generated which includes evaluation of the alternative approachs and should be useful in quickly determining program status at any time.

Summary of Design Alternatives for the Analog Voltage to Duty Cycle Generator

THIN FILM RESISTORS

During the past six months, Westinghouse has developed a production process for thin film tantalum resistors. This process is now being used on the WS 254 product. These resistors could be used to advantage in several divider networks in the present design of the Duty Cycle Generator. They may be trimmed by large current pulses rather than selective bonding as presently planned. The selective bonding approach requires that the integrated resistor be broken into a sufficient number of steps to provide the required resolution. In the case of the divider ratio which sets the reference supply, the $\pm$5% tolerance associated with the reference element must be trimmed out by selective bonding to 0.01%. On a single resistor this would require 500 separate taps, but may be achieved by two resistors in cascade with 20 and 25 taps. However, at best, the approach is awkward and requires a large geometry. In the thin film approach, the approximate resistor ratios may be determined after semiconductor diffusions are complete and further trimming achieved by pulsing the resistors with sufficient current to further oxide their surface and increase resistance.

Presently, most of the frequency tolerance on the time base ($\pm$5%) is taken up by the temperature coefficient of the resistors. This could also be greatly improved in the present design by the use of tantalum resistors for the RC networks. If an analog approach were used the same advantage would be realized

ANALOG RAMP GENERATOR

Our original system proposal considered and rejected the analog approach to ramp generation on the basis that we could not integrate capacitors larger than about 100 pf with a reasonable yield. Our experience with tantalum resistors and recent capacitor research has convinced us that our micro-circuit flexibility could be greatly improved without compromising reliability by using hybrid technology. Generally this technology would not be hybrid in the sense that several separate chips or thin film substrates must be interconnected by bonding. It would merely be another process step added to the many already required to produce a fully integrated circuit. Therefore, the reliability of a monolithic system is preserved while using the additional flexibility of a hybrid system. A block diagram of the complete system using an analog ramp generator is shown in Figure 1. The transfer function of the bistable level detector is shown in Figure 2. The input to the integrator is referenced to +5 volts and therefore its output will follow the path indicated by the arrows in Figure 2. The absolute voltage values of the level detector may be very accurately set by the reference supply so that drift in the operational amplifier does not affect the system accuracy.

A timing and logic diagram is shown in Figure 3. The ramp has actually been replaced by a Triangular Function Generator per the schematic of Figure 4. Linearity of this generator is assured by the current gain of the operational amplifier used as the integrator. Current into the summing point must be balanced by current charging the integrating capacitor and current into the amplifier. Current into the amplifier is constant except for the amount required to move the amplifier output $\pm$ 2 volts. If the D.C. voltage gain of the amplifier is set to 1000 with a fixed feedback resistor (also required for D. C. bias) the maximum differential current into the feedback resistor would be 10^{-3} of the charge current.

ANALOG RAMP GENERATOR (continued)

Differential current into the input pair is even a small part of this since they are being used in a Darlington configuration (in the nano-amp region). Therefore, nonlinearity from this source will be less than 0.2%. The circuit of Figure 4 has been breadboarded and substituted into the existing system. The overall duty cycle nonlinearity (including difference amplifier) was measured at $\pm$0.32%. This performance is well within the limits defined in our First Monthly Progress Report as necessary to meet overall system specifications.

This accuracy also may be quickly approximated by considering that the RC circuit associated with the operational amplifier is charging toward 2000 volts and being reserved after reaching 2 volts.

COMPARISON OF ANALOG AND DIGITAL SYSTEM ACCURACY

Typically, analog systems rely heavily on the characteristics of a few components and become extremely complex when carried to accuracy extremes. Digital systems inherently require a large number of components, but come into their own when high degrees of accuracy are required. The crossover point is usually determined by the system requirements or device limitations.

The overall sensitivity of the Duty Cycle Generator was determined on the basis of acceptable load regulation ($\pm$.5%) and is quite in line with practical degrees of temperature stability ($\pm$.25%) which is a device limitation. The reference element and differential amplifier input pair determine to basic temperature stability of the system. Circuit complexity and accuracy of the remaining blocks must be justified by comparison with these elements.

Matching of the ladder resistors is limited by device technology and was estimated at $\pm$ 0.3%. This limitation might be improved by slightly modified fabrication approaches. However, if this were done, the accuracy of the ladder supplies would have to be improved by further complexity to match the new levels of accuracy. Ultimately, the accuracy of the digital ramp would probably exceed that of the analog triangle, but further refinement does not seem justified based on system requirements and block capabilities.

In order to maximize design flexibility, the combined effect of sensitivity and linearity were limited by Jet Propulsion Laboratory to $\pm$ 3%. This tolerance is spread among several contributing factors between $\pm$0.1% and 0.5% each. This would indicate that design complexity is in line with fundamental technology limitations.

The Triangular Function Generator has been designed to meet the present linearity specification of the Digital Ramp Generator.

COMPARISON OF ANALOG AND DIGITAL SYSTEM ACCURACY (continued)

A summary of all comparisons made in this section are listed in Table 3. In the digital approach, sensitivity is directly related to the auxiliary power supply voltage which has an accuracy of ± 0.3%. This tolerance is determined by the same considerations which determine the threshold accuracy of the Bistable Level Detector in the analog system. Linearity of the digital ramp is related to the ladder ratios (± 0.3%) plus the load regulation of the auxiliary supplies (± .4%). Linearity of the triangle generator is related to the operational amplifier as discussed earlier and will be better than ± 0.5%. Without further modification it would appear that the accuracy of the two approaches are quite comparable.

In this system, component count for equal accuracies favors the analog approach as indicated in Table 1. However, consideration must be given to the types and reliability of the components involved. It turns out here that all of the components except capacitors are quite comparable in reliability (including diodes versus transistors) except the capacitors. The TEOS capacitor used in the binaries would be a prime factor in the yield and reliability of the binaries as would the tantalum capacitor in the analog system. However, the tantalum capacitor will be on a separate chip (or fabricated separately on a single chip) and may be selected from several units if necessary. In fact, if the capacitor were to be moved outside the package, it would require less space than the shaping network contemplated for the difference amplifier (0.05 μF).

As shown in Table 2, the digital approach requires 2 watts of power dissipation even after redesign of the binaries, while the analog approach requires 1.3 watts. 1.3 watts would allow operation in free air, but would probably not be advisable from load regulation consideration. In both systems device dissipation will be somewhat a function of duty cycle (±10%) and would cause drift in the reference element if used in free air.

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COMPARISON OF ANALOG AND DIGITAL SYSTEM ACCURACY (continued)

Chatter in the duty cycle is presently caused and/or magnified by the presence of high frequency spikes in the amplifier and on the ramp. These spikes may be reduced by various methods of ground, power supply isolation and shielding, but will remain a source of potential problem in the digital system.

At this point, it is not clear whether switcing transients within the regulator itself will be adequately ignored by the Duty Cycle Generator but this problem would remain with either the analog or digital ramp. This problem could perhaps be solved by a circuit which would limit the output to one pulse per cycle (lock-out). Frequency shaping of the amplifier for loop stabilization is limited by increased sensitivity to high frequency spikes (in the case of lead networks). False triggering of the output logic will be corrected in either system by emitter follower decoupling of the 2.5kc binary.

In the digital system, a minimum of two chips are needed, considering only the process differences required for high speed digital transistors and high beta analog units. Yield requirements may increase the number.

The analog system requires a minimum of one chip, but will be more practical from the fabrication point of view, if at least two are used. Again, yield requirements may increase this number. There is very little difference in the number of jumper bonds since they would be used primarily between functional blocks when necessary.

FUTURE SCHEDULE

Figure 9 is a reduction of our program schedule which will be updated weekly with percent completion tabulations. The schedule has been designed around the manpower currently available and in anticipation of normal problems. Use of an "Insta-Circuit" prototype phase should insure that time spent in the monolithic block layout and mask making phase will be on a proven integrated circuit design. Insta-Circuit is a single die containing an array of integrated components, which may be interconnected by ball bonding contact pads and aluminum strips. A brief description of these units has been included in Figures 5 through 8.

COMPARATIVE PARTS COUNT

DESCRIPTION	Capacitor	Transistors	Diodes	Resistors	TOTAL
Blocks associated with DIGITAL APPROACH only					
Time Base	2	2		4	
Binary Counter	18	18	98	72	
Ladder		16		57	
Ladder Supplies		6		12	
	20	42	98	145	= 305
ANALOG & DIGITAL Blocks					
Difference Amplifier	3	12	4	22	
Reference Supply	2	4	5	7	
Comparator		4	3	7	
Output Logic		4	6	6	
	5	24	18	42	= 89
ANALOG only Blocks					
Triangle Gen.	2	19	7	28	
2.5 kc Binary	2	2	12	8	
	4	21	19	36	= 80
DIGITAL TOTAL	25	66	116	187	= 394
ANALOG TOTAL	9	45	37	78	= 169
DIFFERENCE	16	21	79	109	= 225

57% Reduction in Parts Count

POWER REQUIREMENTS

DIGITAL ONLY

TIME BASE	15 ma	
BINARY COUNTER	20	new design
LADDER	0	old design = 60
LADDER SUPPLIES	20	
	55	

ANALOG AND DIGITAL

DIFFERENCE AMPLIFIER	15	
REFERENCE SUPLLY	25	
COMPARATOR	2	
OUTPUT LOGIC	6	
	48	

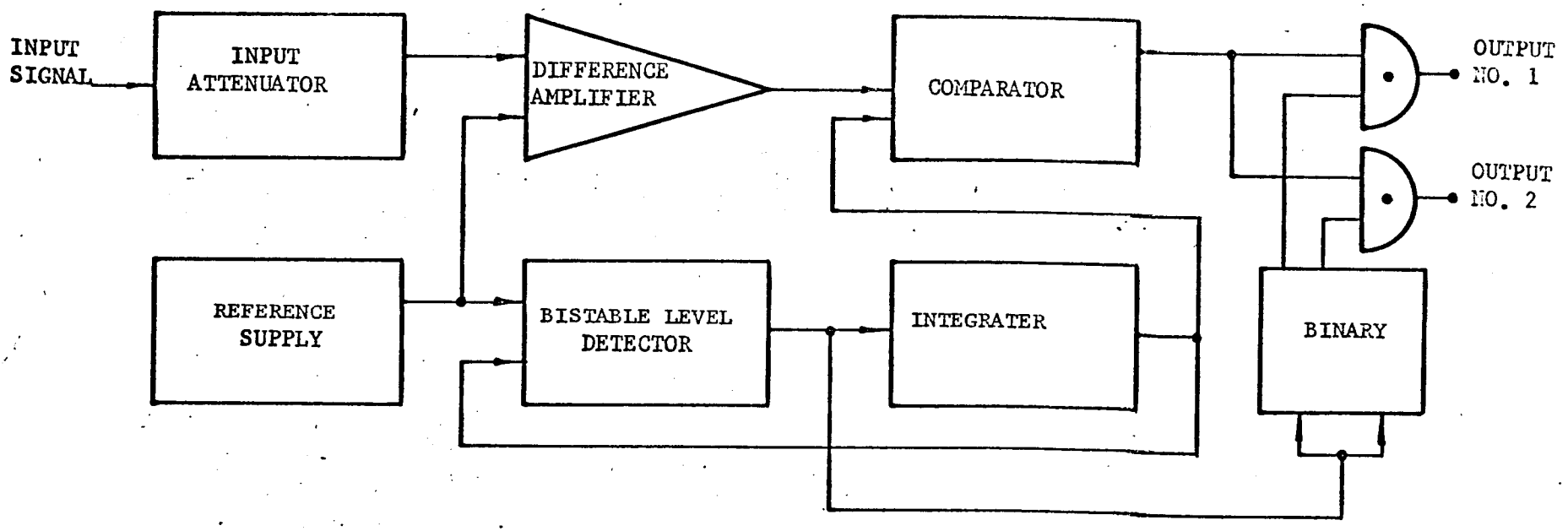
ANALOG ONLY

TRIANGLE GENERATOR	15	
2.5 kc BINARY	2	
	17	

DIGITAL TOTAL	103	= 2.06 watts
ANALOG TOTAL	65	= 1.30 watts
DIFFERENCE	38	= 37% reduction

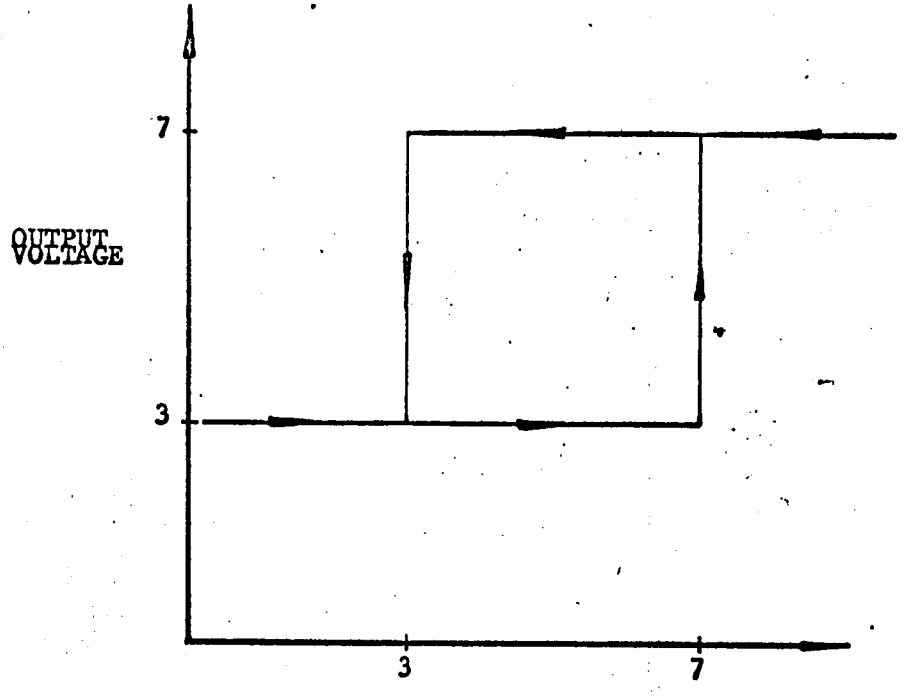
COMPARISON OF ANALOG AND DIGITAL SYSTEMS

FACTOR	DIGITAL APPROACH	ANALOG APPROACH
ACCURACY:		
Linearity	±0.3% ladder matching	± 0.5%
	±0.4% P.S. regulation	
Sensitivity	±0.3%	± 0.3%
Power Dissipation	2.0 watts	1.3 watts
HIGH FREQUENCY SPIKES:		
Ramp	Faster switching	None required
Amplifier	Separation Power Supply	None required
Signal	Lock-out etc.	Lock-out etc.
Frequency Shaping	Limited by noise rejection	Open loop rolloff
Complexity	Analog system requires 60% fewer components	
Number of Chips	2 processes	1 process



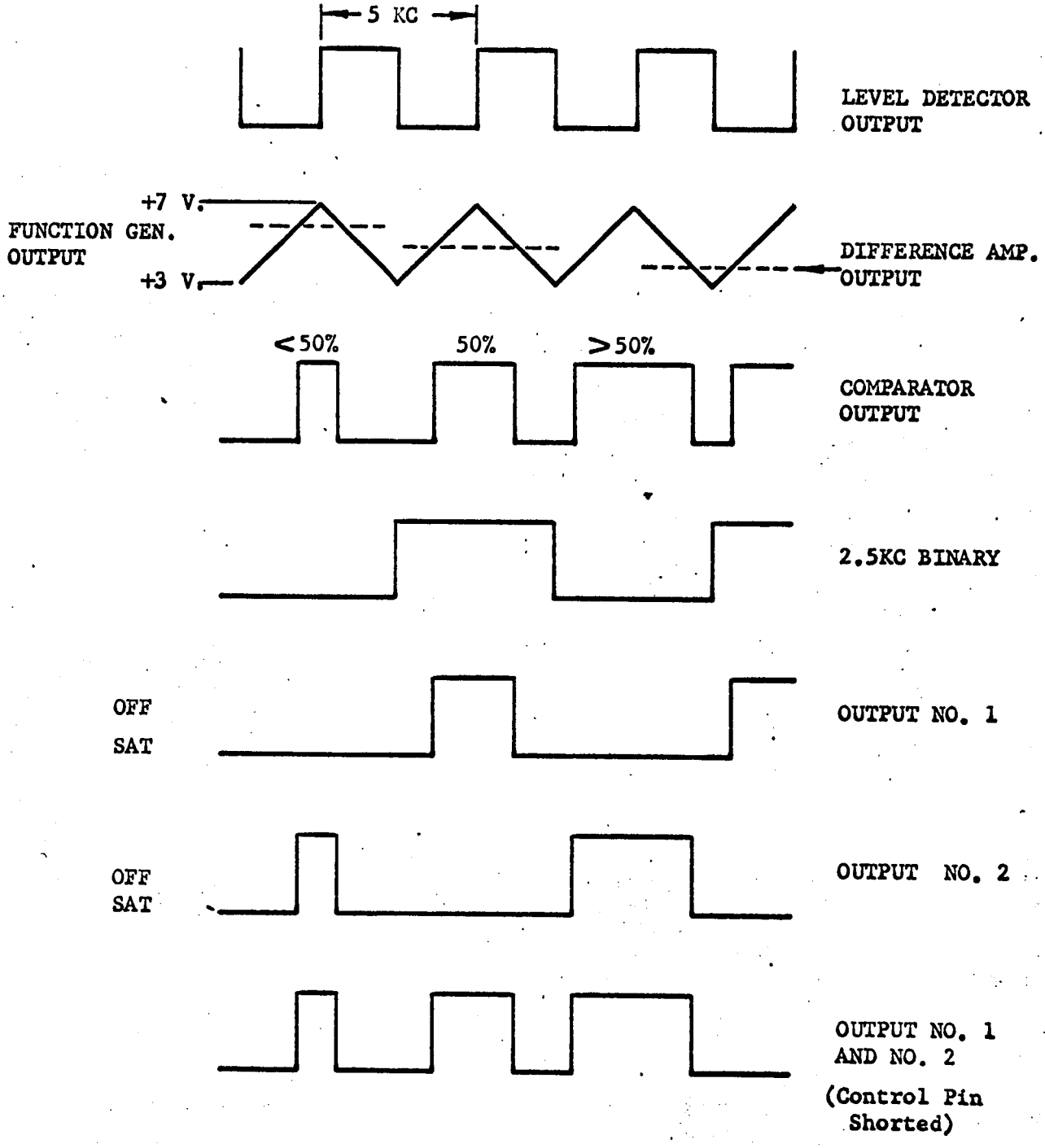
ANALOG SYSTEM BLOCK DIAGRAM

FIG. 1



BISTABLE LEVEL DETECTOR
TRANSFER FUNCTION

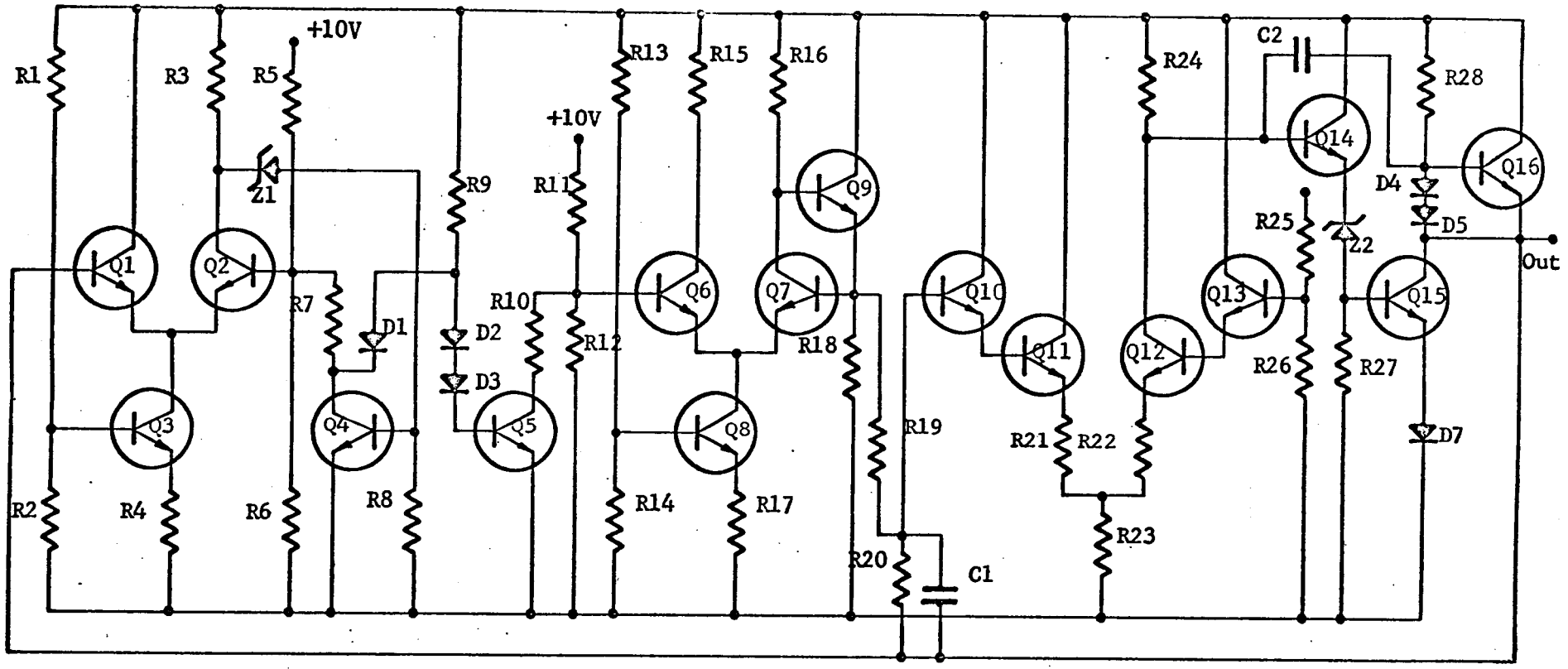
FIG. 2



TIMING AND LOGIC DIAGRAM

FIG. 3

+20V ± 1V



R1=9.1K
R2=1K
R3=13K
R4=1.3K
R5=3K
R6=7.5K
R7=1.5K
R8=6.8K
R9=20K
R10=1.5K

R11=3K
R12=7.5K
R13=9.1K
R14=1K
R15=30K
R16=30K
R17=1.3K
R18=1K
R19=1K
R20=1M

R21=510
R22=510
R23=3.0K
R24=20K
R25=5K
R26=5K
R27=10K
R28=20K
C1=0.05
C2=10pf

Figure 4

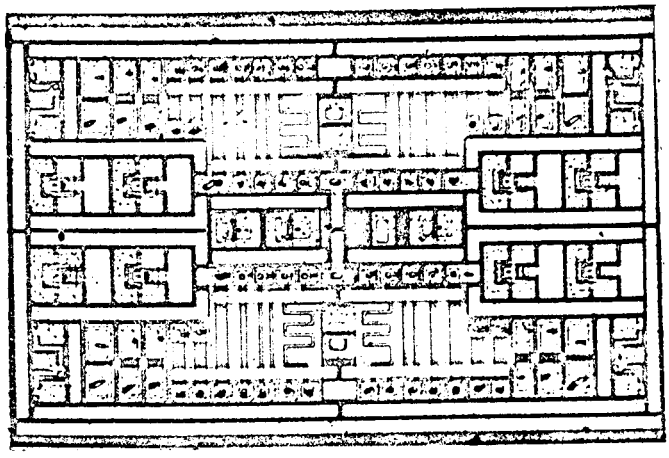
Insta-Circuit Section

WESTINGHOUSE ELECTRIC CORPORATION
MOLECULAR ELECTRONICS DIVISION

PRELIMINARY SPECIFICATION

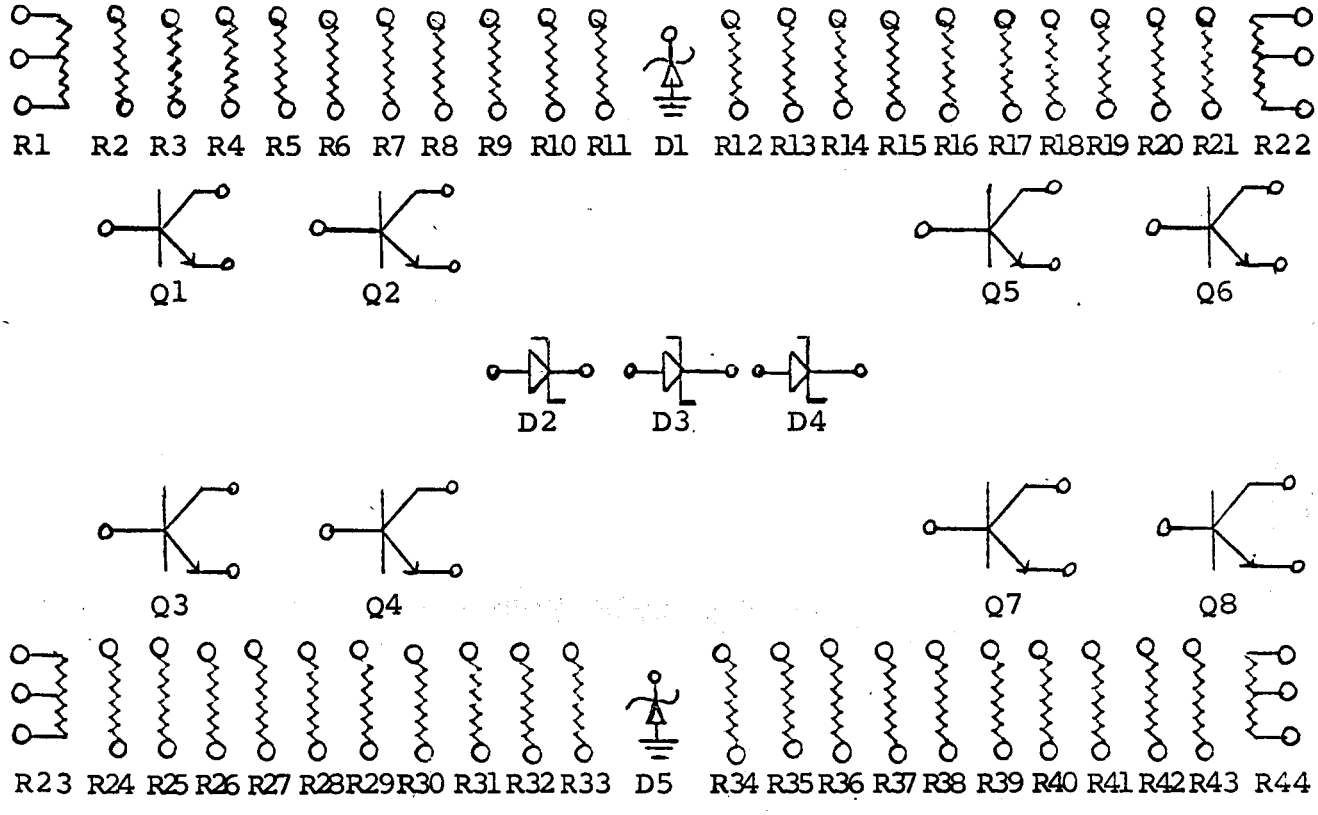
INSTA-CIRCUIT - WS177Q, WS177T

MONOLITHIC SILICON BREADBOARD



The WS177 is a silicon monolithic circuit die mounted in an unlidded 1/4" x 1/4" 14-lead flat pack or 10-pin TO-5 header. The device is intended for use in silicon breadboarding applications and is designed to provide a fast, economical method of evaluating feasibility of custom integrated circuit. The "Insta-Circuit" concept reduces design time to a matter of hours, minimizes difficult jumper bonds, and permits freedom of design changes.

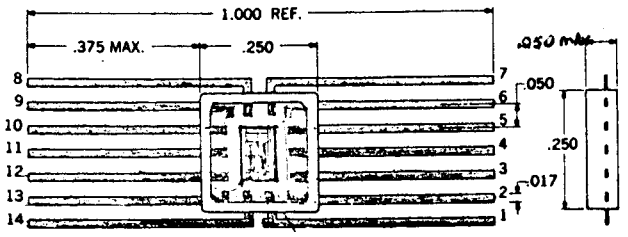
EQUIVALENT CIRCUIT

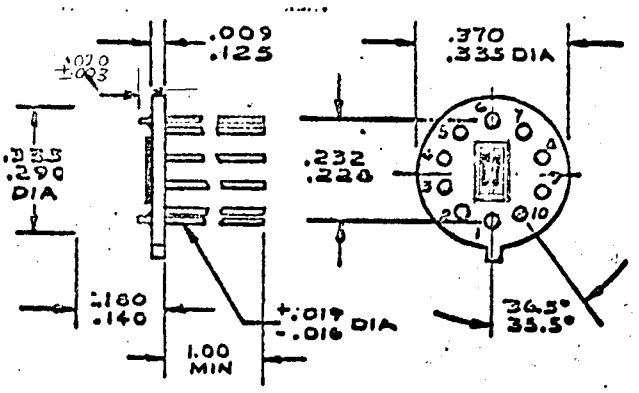


Q-Style Package

T-Style Package

Q style FLAT-PAK (EIA TO-86)





APPLICATIONS

Amplifiers
Oscillators
Level Detectors
Regulators
Voltage Comparators
Demodulators
Digital Logic
(slow-medium speed)

DICE SPECIFICATIONS

Length:	124 mils
Width:	86 mils
Max. Dis.:	250 mw

DESIGN AND USE

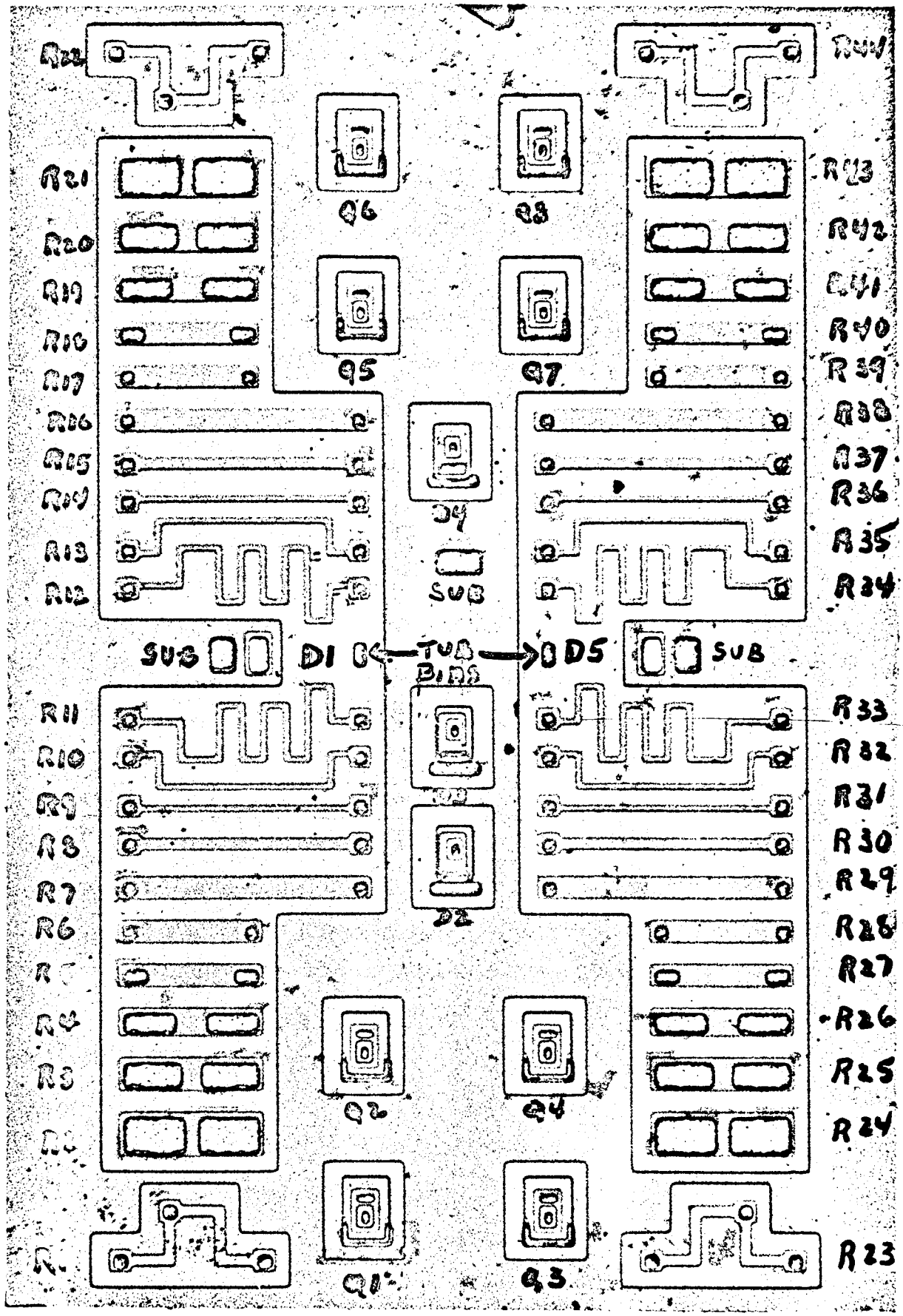
Insta-Circuits are monolithic dice containing all the components of integrated microcircuits. The aluminum interconnect pattern is so arranged with its constant one mil separation, that a simple ball or wedge bond acts as a shorting bar to complete the circuit. After the bond is made, removal of the excess pigtail in no way impairs the solidity of the bond itself. (See Fig. 1).

The basic die consists of four groups of diffused silicon resistors, eight planar transistors and five zener diodes.

Each set of resistors ranges from 100 ohms to 20K ohms in a 8-4-2-1 coded relationship, allowing formation of any resistance value from 100 ohms to 46K ohms in 100 ohm increments by a series connection. Parallel combinations can provide numerous other resistor values. Absolute values of each individual resistor is less than ± 20% with temperature coefficients of approximately + 2000 P.P.M. Tracking between two resistors over the normal temperature range is approximately 0.2%.

Insta-Circuits are supplied in open packages along with their lids and solder preforms. Lid sealing may be accomplished on a simple hot plate if a commercial sealer is not available. Prior to seal, it is advisable to thoroughly clean the die with alcohol or similar cleansing agent and bake in an inert gas atmosphere at 200°C for approximately eight hours.

It is further recommended that open package units be held in a desiccator until sealed.



WS177 DIE COMPONENT LAYOUT

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COMPONENT CHARACTERISTICS

RESISTORS (25°C)

R1, R22, R23, R44	50Ω	tapped at 20Ω ± 20% ± 5% match
R2, R21, R24, R43	100Ω	± 20% ± 5% match
R3, R20, R25, R42	200Ω	" "
R4, R19, R26, R41	400Ω	" "
R5, R18, R27, R40	800Ω	" "
R6, R17, R28, R39	1000Ω	" "
R7, R16, R29, R38	2000Ω	" "
R8, R15, R30, R37	4000Ω	" "
R9, R14, R31, R36	8000Ω	" "
R10, R13, R32, R35	10,000Ω	" "
R11, R12, R33, R34	20,000Ω	" "

TRANSISTORS (25°C)

Q1 to Q8 NPN Epitaxial Planar Type (non-gold doped)
Beta 40-120
I_C = 1MA, V_{CE} 5V
BV_{CEO} > 30V
BV_{CBO} > 60B
BV_{EBO} 8.2V ± 5%
V_{CE} (SAT) 0.25V
I_C = 5MA, I_b = 0.5MA
C_{OB} < 3 pf
F_T > 200 Mhz
PNP Parasitic Beta 0.05 Typ

DIODES (25°C)

D1, D5	5.8V Zener Diode to Substrate ± 5%
D2, D3	5.8V Zener Diode, floating ± 5%
D4	8.2V Zener Diode, floating ± 5%

TESTING

Because of the impracticability of individually testing each of the 61 components on the "Insta-Circuit" die, a simple probe test was found necessary. The test consists of measuring a high value and a low value resistor for their absolute values, the breakdown voltage of one zener diode, and the complete beta and breakdown characteristics of two transistors. Although 100% testing is not performed, this test method does assure a high degree of confidence in the quality of the untested components.

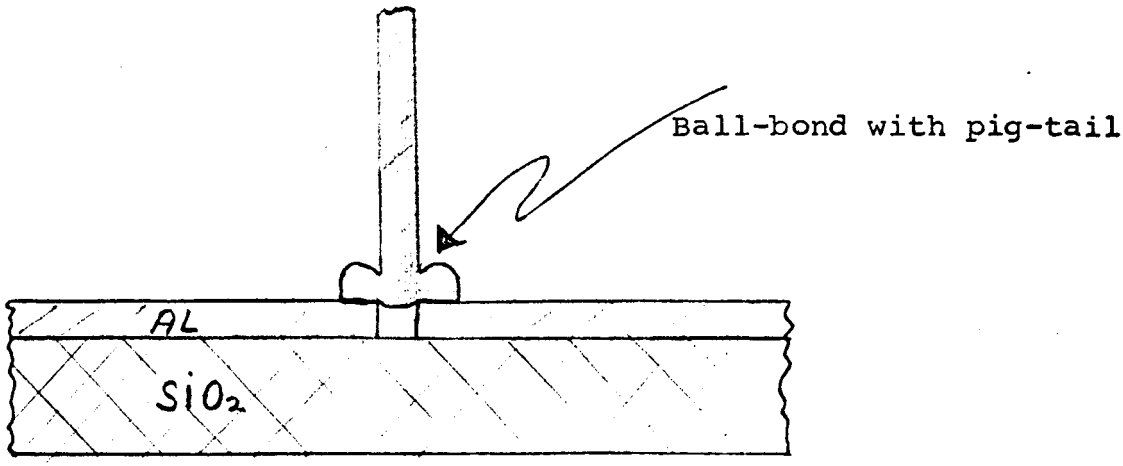

Fig. 1 (A)

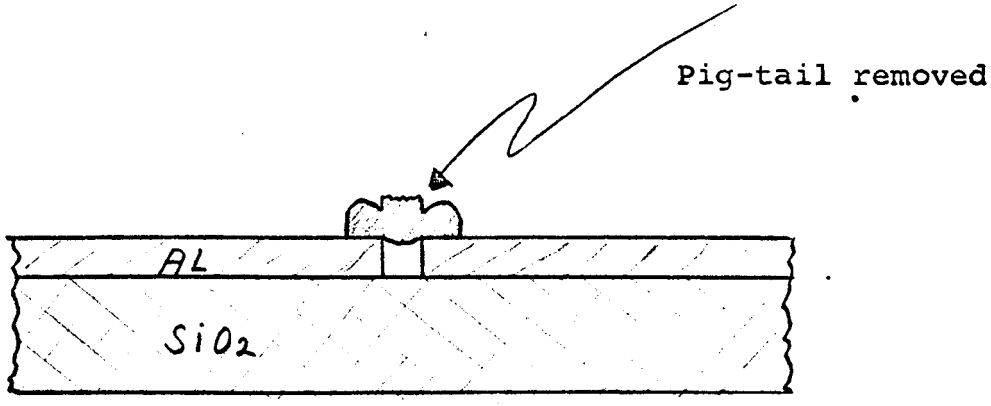

Fig. 1 (B)

ILLUSTRATION OF BALL-BOND AS SHORTING BAR

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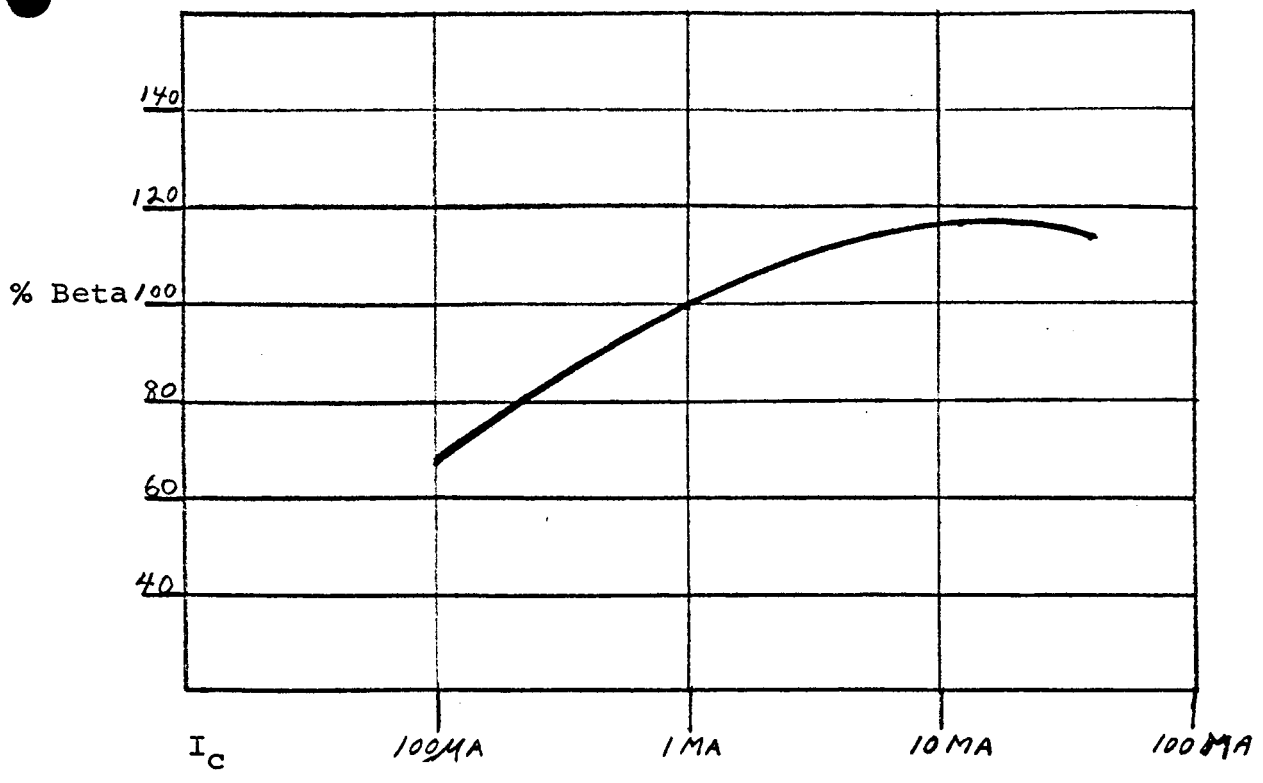
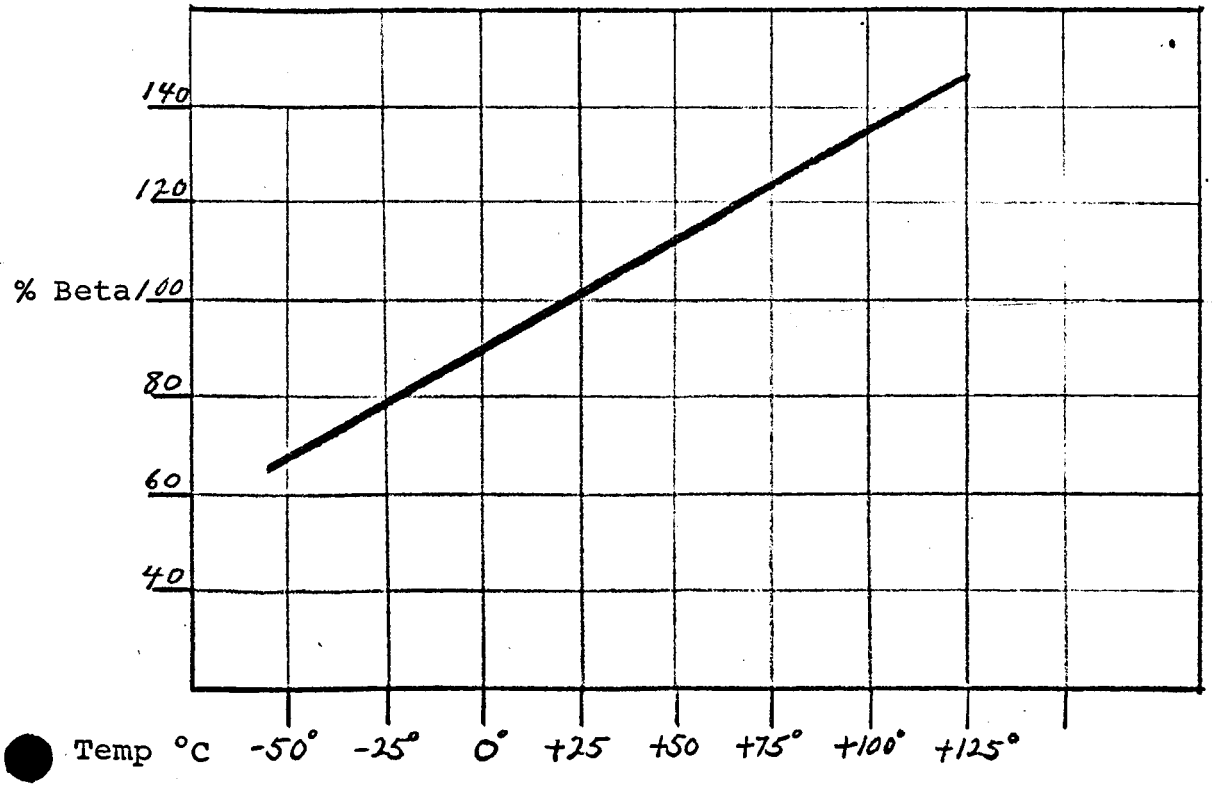
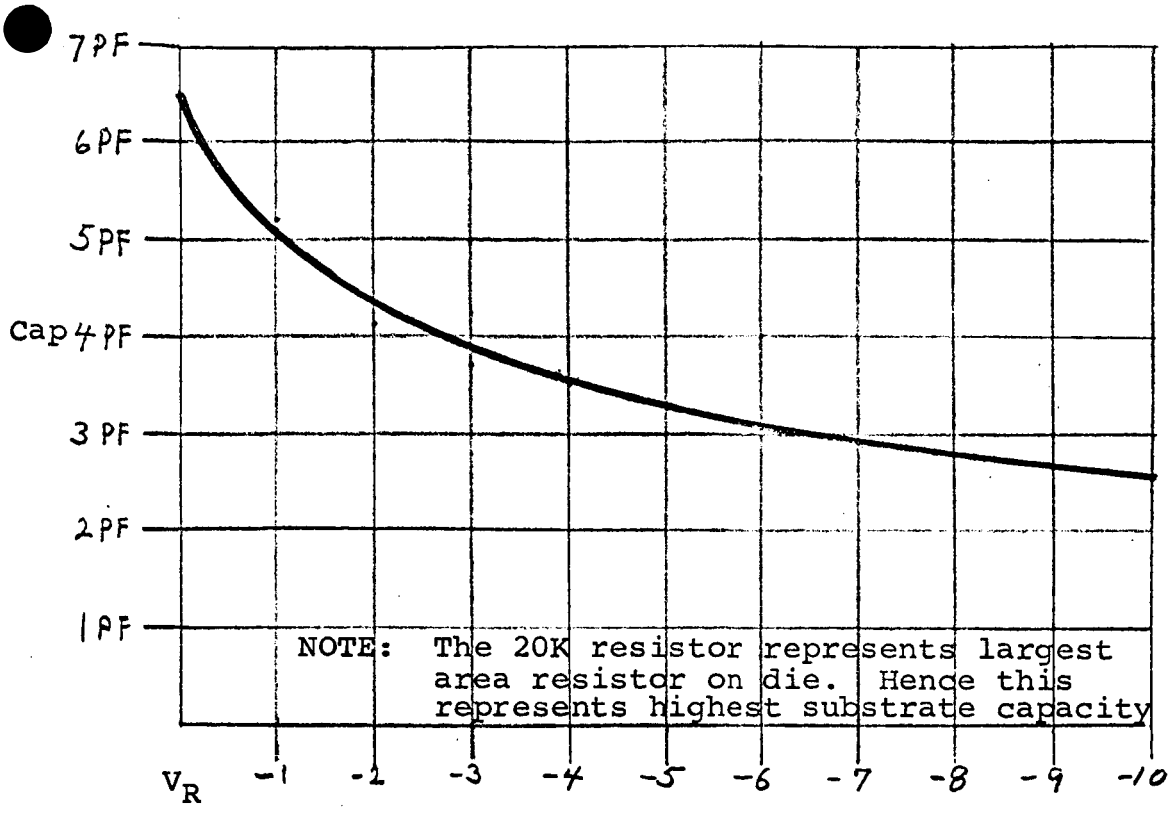


WS177 TRANSISTOR BETA vs COLLECTOR CURRENT AT 25°C

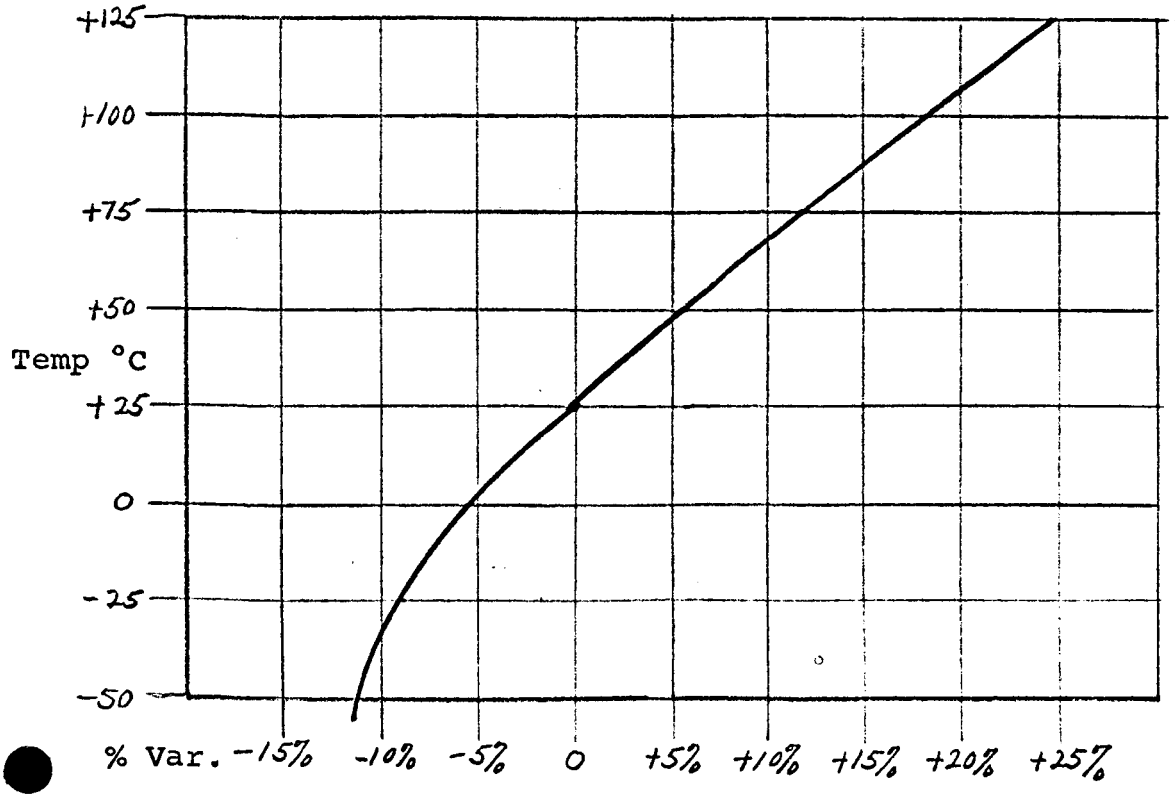


WS177 TRANSISTOR BETA vs TEMPERATURE AT I_C = 1MA

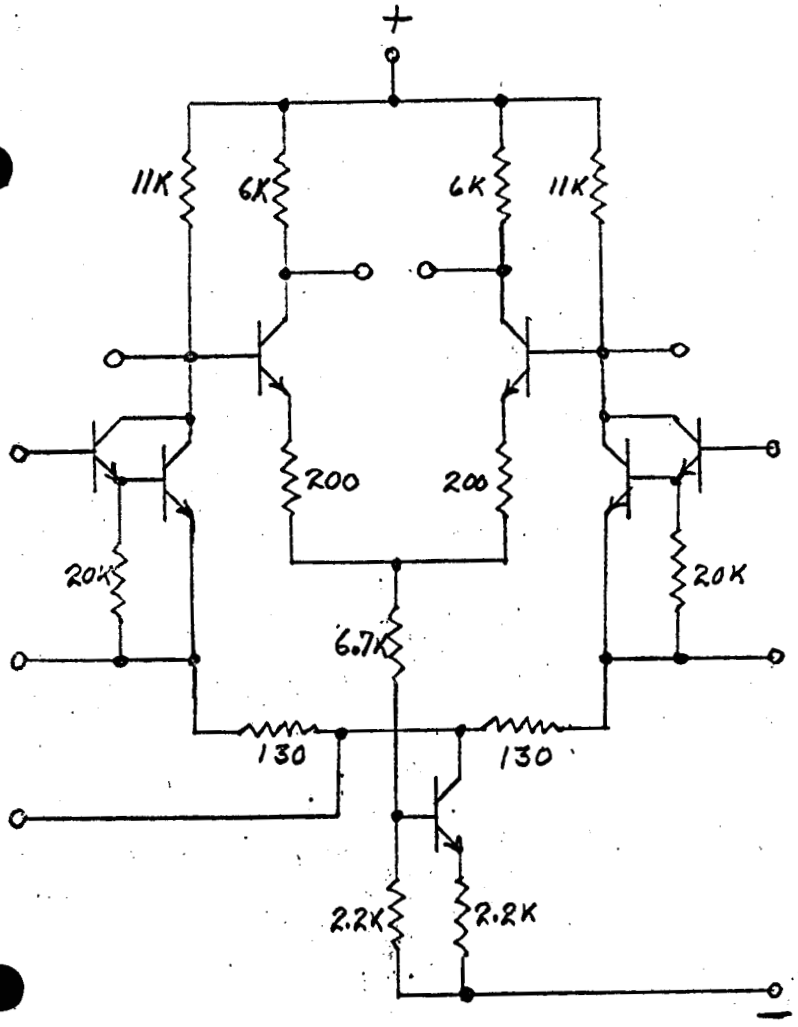
23



20K RESISTOR CAPACITY TO N TUB vs REVERSE BIAS AT 25°C



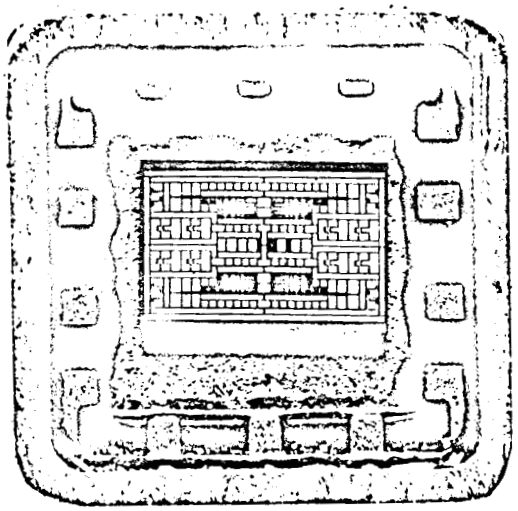
TYPICAL WS177 RESISTOR TEMPERATURE COEFFICIENT



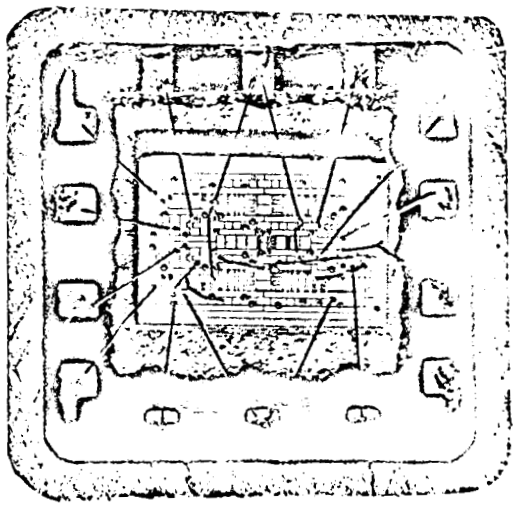
USE OF WS177 8-4-2-1 CODED RESISTORS.

11K	=	10K +1K (Series)
6K	=	4K + 2K (series)
20K	=	20K
200	=	200
6.7K	=	20K + 10K (Parallel)
130	=	130
2.2K	=	2K + 200 (Series

Resistor N tubs reverse biased to $+V_{CC}$, substrate biased to $-V_{CC}$



WS177 DIE IN Q PACK



COMPLETED CIRCUIT USING "INSTA-CIRCUIT" TECHNIQUE

EVOLUTION OF INSTA-CIRCUIT FROM SCHEMATIC TO PROTOTYPE DEVICE

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Tantalum Film Capacitors
Reliability

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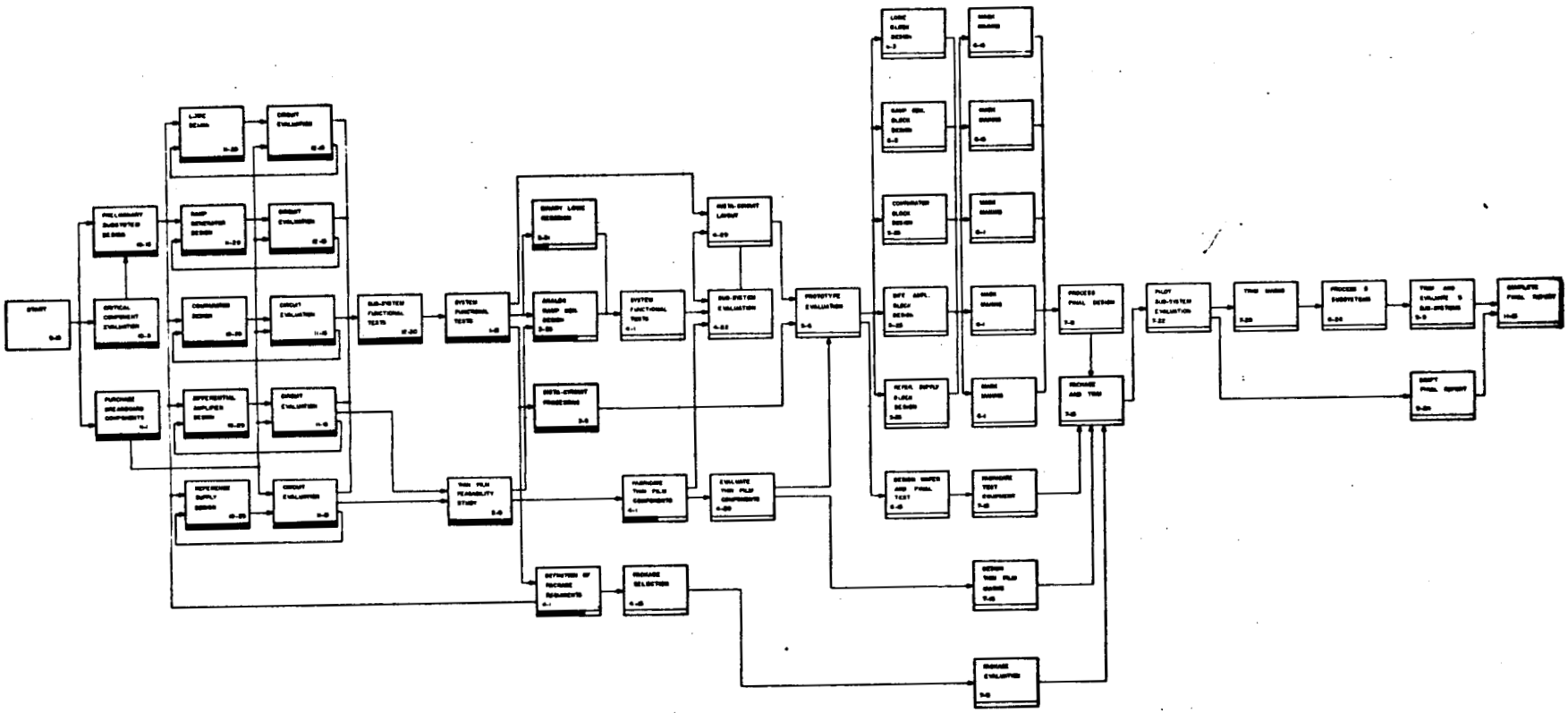

ANALOG VOLTAGE TO DUTY CYCLE GENERATOR PROGRAM SCHEDULE

JPL CONTRACT NUMBER 955305